The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1 - 46 (Previously Cancelled).

47. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a first bit line connected to said first memory cell section;

a second bit line connected to said second memory cell section, being different from said first bit line; and

~~a latch circuit having~~ a common ~~node~~ latch circuit connected to one ends of said first and second bit lines;

wherein first program /read data of said first memory cell is latched in said common latch circuit, while second program /read data of said second memory cell is held by said second bit line.

48. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a first bit line connected to said first memory cell section;

a second bit line connected to said second memory cell section, being different from said first bit line; and

~~a latch circuit having~~ a common ~~node~~ latch circuit connected to one ends of said first and second bit lines;

wherein

said first and second memory cells are programmed substantially simultaneously; and

while said program voltage is supplied to said second memory cell, a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said common latch circuit, and while said program voltage is supplied to said first memory cell, a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said latch common circuit.

49. (Previously Presented) A nonvolatile semiconductor memory according to claim 48,

wherein

while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second bit line, and

while said program voltage is supplied to said first memory cell, program data of said first memory cell is held by said first bit line.

50. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a second memory cell section including a second memory cell;

a first bit line connected to said first memory cell section;

a second bit line connected to said second memory cell section, being different from said first bit line; and

~~a latch circuit having a~~ common ~~node~~ latch circuit connected to one ends of said first and second bit lines;

wherein

said first and second memory cells are programmed substantially simultaneously;

while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second bit line, and while said program voltage is supplied to said second memory cell, the program data of said first memory cell held by said first bit line is latched in said common latch circuit and a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said common latch circuit;

while said program voltage is supplied to said first memory cell, program data of said first memory cell is held by said first bit line, and while said program voltage is supplied to said first memory cell, the program of data said second memory cell held by said second bit line is latched in said common latch circuit and a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said common latch circuit.

51. (Original) The nonvolatile semiconductor memory according to claim 47, wherein

said first memory cell and said second memory cell are connected to different word lines.

52. (Original) The nonvolatile semiconductor memory according to claim 48,

wherein

said first memory cell and said second memory cell are connected to different word lines.

53. (Original) The nonvolatile semiconductor memory according to claim 49, wherein

said first memory cell and said second memory cell are connected to different word lines.

54. (Original) The nonvolatile semiconductor memory according to claim 50, wherein

said first memory cell and said second memory cell are connected to different word lines.

55. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a first bit line connected to said first memory cell section;

a second bit line, being different from said first bit line; and

~~a latch circuit having a~~ common ~~node~~ latch circuit connected to one ends of said first and second bit lines latching program / read data;

wherein

said program / read data of said first memory cell is held by said second bit line.

56. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a first bit line connected to said first memory cell section;

a second bit line, being different from said first bit line; and

~~a latch circuit having a~~ common ~~node~~ latch circuit connected to one ends of said first and second bit lines, latching program / read data;

wherein

while a program voltage is supplied to said first memory cell, program data of said first memory cell is held by at least one of said first and second bit lines;

after said program voltage is supplied to said first memory cell, said common latch circuit is electrically connected to said second bit line and the program data of said first memory cell held by said second bit line is latched in said common latch circuit; and

a verify read operation to verify whether said first memory cell has been sufficiently

programmed, is carried out using said program data latched in said common latch circuit.

57. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first memory cell section including a first memory cell;

a first bit line connected to said first memory cell section;

a second bit line;

a second memory cell section including a second memory cell;

a third bit line connected to said second memory cell section;

a fourth bit line; and

~~a latch circuit having~~ a common ~~node~~ latch circuit connected to one ends of said first, second, third and fourth bit lines, latching program/read data of at least one of said first and second memory cells;

wherein

said first, second, third and fourth bit lines are different from each other;

said first and second memory cells are programmed substantially simultaneously, program data of said first memory cell is held by at least one of said first and second bit lines, and program data of said second memory cell is held by at least one of said third and fourth bit lines while a program voltage is supplied to said first and second memory cells;

a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out by said common latch circuit, and program data of said second memory cell is held by said fourth bit line while conducting the verify read operation of said first memory cell; and

said common latch circuit and said fourth bit line are electrically connected to each other, after the program data of said second memory cell held by said fourth bit line is latched in said common latch circuit, a verify read operation to verify whether said second memory cell has been sufficiently programmed, is carried out using the program data of said second memory cell held by said common latch circuit, and while conducting a verify read operation of said second memory cell, the program data of said first memory cell is held by said second bit line.

58. (Previously Presented) The nonvolatile semiconductor memory according to claim 57, wherein

said first and second memory cells are connected to a same word line.

59. (Previously Presented) The nonvolatile semiconductor memory according to claim 55, wherein

while said program / read data is held by said first or second bit line, a potential of a bit line adjacent to said first or second bit line is set at a fixed potential.

60. (Original) The nonvolatile semiconductor memory according to claim 59, wherein

said fixed potential is a ground potential or a power supply potential.

61. (Canceled)

62. (Previously Presented) The nonvolatile semiconductor memory according to claim 56, wherein

while said program / read data is held by said first or second bit line, a potential of a bit line adjacent to said first or second bit line is set at a fixed potential.

63. (Original) The nonvolatile semiconductor memory according to claim 62, wherein

said fixed potential is a ground potential or a power supply potential.

64. (Canceled)

65. (Previously Presented) The nonvolatile semiconductor memory according to claim 57, wherein

while said program / read data is held by said first, second, third or fourth bit line, a potential of a bit line adjacent to said first, second, third or fourth bit line is set at a fixed potential.

66. (Previously Presented) The nonvolatile semiconductor memory according to claim 65, wherein said fixed potential is a ground potential or a power supply potential.

67-81. (Canceled)